Remarks:

Reconsideration of the application is requested.

Claims 1-10, 15 and 17 are now in the application. Claim 15 has been amended and claim 17 has been added. Claims 11-14 and 16 have been cancelled. Claims 1-10 have been withdrawn from further consideration at this time.

In item 3 on page 2 of the above-identified Office action, Claims 11-14 have been rejected as being anticipated by Komata et al. (Japanese Application JP 2-15897) under 35 U.S.C. § 102(b). Claims 11-14 have been cancelled.

In item 4 on pages 2-3 of the above-identified Office action, Claims 11-13 have been rejected as being anticipated by Katz et al. (US Pat. No. 5,197,654) under 35 U.S.C. § 102(b). Claims 11-13 have been cancelled.

In item 6 on pages 3-4 of the above-identified Office action, Claims 15-16 have been rejected as being unpatentable over Inasaka (US Pat. No. 5,585,138) in view of Komata et al. under 35 U.S.C. § 103(a).

The rejection has been noted and claim 15 has been amended in an effort to even more clearly define the invention of the instant application. More specifically, the features of

claims 16 and 7 have been added to claim 15. Claim 16 has been cancelled.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 15 calls for, inter alia:

> said solder containing a gold-tin compound (AuSn) with a hypereutectic Sn concentration and forming a ***layer having a thickness of from about 1 μm to about 2 μm***.

Inasaka discloses a micropin array and a production method therefor. Fig. 7 of Inasaka shows a solder 7, a substrate 9 and a semiconductor chip 8. However, in Inasaka, contrary to the invention of the instant application, the semiconductor chip 8 is not directly connected to the substrate 9, but via a micro array 5.

Komata et al. show in Figs. 1-3 a method for producing a solder 13 which contains two components: gold and tin. The tin content is 12-37% by weight, thus the solder has a hypereutectic concentration of tin. A person skilled in the art might provide a hypereutectic concentration of tin, as disclosed in Komata et al., for the solder 7 in Inasaka. However, a person skilled in the art does not have any motive to eliminate the micropin array 5 of Inasaka.

Furthermore, neither Komata et al. nor Inasaka has disclosed a solder which forms "***a layer having a thickness of from about 1 μm to about 2 μm***", as recited in claim 15 of the instant applicaiton.

In summary, the semiconductor component according to the invention of the instant application distinguishes itself from the prior art in that a semiconductor chip is directly (without a micro array) attached to a substrate via a gold-tin-solder with a hypereutectic Sn concentration and a layer thickness of about 1-2 μm. Such a connection between a semiconductor chip and a substrate has proven to be particularly strong and a chip break will practically not occur (see page 4, line 19 to page 6, line 10 of the specification for a detailed description of the advantages of the invention of the instant application).

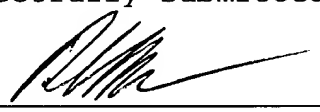
It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 15. Claim 15 is, therefore, believed to be patentable over the art.

In view of the foregoing, reconsideration and allowance of claims 1-10, 15 and 17 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate a telephone call so that, if possible, patentable language can be worked out.

Please charge any other fees which might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,



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January 24, 2002

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Marked-Up Version of the Amended Claims:

Claim 15(amended). A semiconductor component, comprising:

a solder containing at least two components with at least two metal-containing constituents including a first constituent X being formed of a precious metal and a second constituent Y being consumed during a soldering operation by one of reacting and being dissolved in materials which are to be joined, and said solder having a hypereutectic concentration of said second constituent Y;

a substrate; and

a semiconductor chip secured to said substrate by one of alloying and brazing using said solder,

said solder containing a gold-tin compound (AuSn) with a hypereutectic Sn concentration and forming a layer having a thickness of from about 1 μm to about 2 μm.